LAr TPC Electronics CMOS Lifetime at 300 K and 77 K and Reliability Under Thermal Cycling

Shaorui Li, Jie Ma, Gianluigi De Geronimo, Hucheng Chen, and Veljko Radeka

***Abstract*—A study of hot-carrier effects (HCE) on the 180-nm CMOS device lifetime has been performed at 300 K and 77 K for Liquid Argon Time Projection Chamber (LAr TPC). Two different measurements were used: accelerated lifetime measurement under severe electric field stress by the drain-source voltage V_{ds}, and a separate measurement of the substrate current as a function of $1/V_{ds}$. The former verifies the canonical very steep slope of the inverse relation between the lifetime and the substrate current, and the latter confirms that below a certain value of V_{ds} a lifetime margin of several orders of magnitude can be achieved for the cold electronics TPC readout. The low power ASIC design for LAr TPC falls naturally into this domain, where hot-electron effects are negligible. Lifetime of digital circuits (ac operation) is extended by the inverse duty factor $1/(f_{clock}t_{eff})$ compared to dc operation. This factor is large (> 100) for deep submicron technology and clock frequency needed for TPC readout. As an additional margin, V_{ds} may be reduced by $\sim 10\%$. Extremely low failure rate (incidence) in previous large experiments demonstrates that surface mount circuit board technology withstands very well even multiple abrupt immersion in liquid nitrogen applied in board testing, and that the total failure incidence in continuous operation over time is very low.**

***Index Terms*— Cryogenic electronics, hot carriers, lifetime.**

I. Introduction

THE Liquid Argon Time Projection Chamber (LAr TPC) technology offers extraordinarily precise event reconstruction, particle identification, and scalability to very large detectors for neutrino physics and proton decay [1]. The challenge of electronics in this application is the cryogenic operation of all components immersed in LAr at about 87 K, with a requirement to function continuously and unattended for a long time ($>$ 10-20 years).

Most of the major failure mechanisms, such as electro-migration, stress migration, time-dependent dielectric breakdown, negative-bias temperature instability, and thermal cycling, are strongly temperature dependent and become negligible at cryogenic temperature [2], [3], [4]. The only relevant mechanism that may substantially affect the lifetime of CMOS (Complimentary Metal-Oxide-Semiconductor) devices when operating at cryogenic temperature is the degradation due to impact ionization, which causes interface state generation and oxide trapped charge. The degradation affects the device's transconductance, output resistance, and threshold voltage [5], [6], and mainly concerns n-channel devices (NMOS). The p-channel devices (PMOS), affected by a similar degradation mechanism [7], [8], typically exhibit a lifetime one or two orders of magnitude longer than that of the n-channel devices [9], and do not represent a concern in our case. This aging mechanism does not result in sudden device failure. The amount of impact ionization depends on the operating point of the device, reaching the maximum for minimum channel length devices operating at the maximum drain-source voltage (recommended by the foundries) and at gate-source voltage about half of that. Under these conditions, the foundries guarantee at room temperature a lifetime of about 10 years (usually under the worst operating conditions for aging), where lifetime is defined as 10% reduction of the device transconductance. For a device operating at cryogenic temperatures the amount of impact ionization at equal operating point increases, thus decreasing its lifetime. An increase in the substrate (bulk) current, with corresponding decrease in lifetime has been reported for temperatures in the 80 K range [6].

The purpose of our study and the test program had been to try to establish with confidence some lifetime estimates for the CMOS circuits to be operated in LAr. This study and the experiments with devices in TSMC 180-nm CMOS process show that the lifetime at low temperature is limited by a predictable and a very gradual degradation (aging) mechanism which can be controlled in the circuit design. A lifetime at 77 K equal to that at 300 K is achieved by reducing the drain-source voltage by less than 10%. In this study we have been following the basics established in the literature (e.g. [5]), and the practices adopted more recently [6], as well as by CMOS foundries. The background radiation in the experiments (neutrino and dark matter physics studies) where the CMOS circuits will be operated in cryogenic liquids is negligible compared to the radiation at accelerators (e.g., LHC). Thus the combined effects of ionizing radiation and hot carrier stressing [10], [11] have not been included in this study.

II. Overview of Basics on Hot-Carrier Effects and CMOS Lifetime

In any NMOS device electrons can become "hot" at any temperature, by attaining energy $E > kT$, where k is Boltzmann constant, and T is the temperature. With the MOS technology scaling this takes place at lower and lower drain voltages as the

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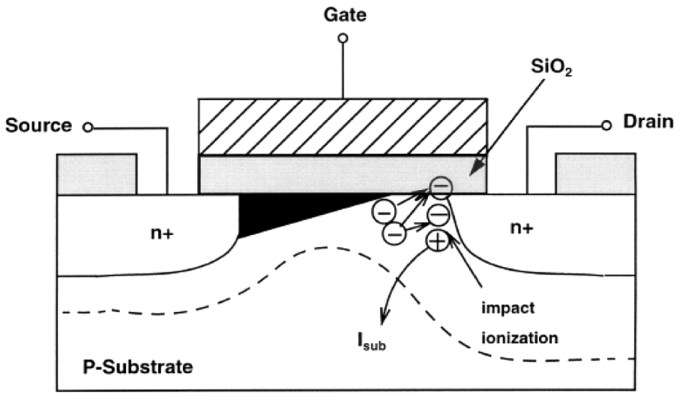

Fig. 1. Schematic representation of impact ionization by hot electrons in the channel of an NMOS device. The holes produced by impact ionization constitute the substrate current.

channel length is decreased. Some hot electrons exceed the energy required to create an electron-hole pair, $\varphi_i \approx 1.3$ eV [12], resulting in *impact ionization* (see Fig. 1). Electrons proceed to the drain. The holes drift to the substrate. The substrate current can be expressed as [5]

$$I_{sub} = C_1 I_{ds}\, e^{-\varphi_i / q\lambda E_m} \tag{1}$$

where C_1 is a constant, I_{ds} is the drain-source current, q is the electron charge, λ is the electron mean free path, and E_m is the channel electric field which is proportional to the difference between drain-source voltage and the pinch-off voltage, i.e. $E_m \propto (V_{ds} - V_{dsat})$.

A very small fraction of hot electrons exceeds the energy required to create an *interface state* (e.g. an acceptor-like trap), in the $\mathrm{Si-SiO_2}$ interface, $\varphi_{it} \geq 3.7$ eV, for electrons (~ 4.6 eV for holes), also shown in Fig. 1. This causes a change in the transistor characteristic (e.g. transconductance, threshold, and intrinsic gain). The changes in different parameters are correlated [5], [9]. The time required to change any important parameter monotonically by a specified amount, e.g. transconductance by -10%, is defined as the device lifetime. It can be calculated as [5]

$$\tau = C_2 \frac{W}{I_{ds}} e^{\varphi_{it} / q\lambda E_m} \tag{2}$$

where C_2 is a constant and W is the channel width.

It has been widely recognized in the literature (e.g. [5], [6]) that substrate current is a monitor for all hot-electron effects and it is the best predictor of device lifetime, because both classes of observable hot electron effects (electrical and optical) are driven by a common driving force, the channel electric field, or more specifically the maximum channel electric field E_m, which occurs at the drain end of the channel. The substrate current I_{sub} is connected to the lifetime τ (defined by any arbitrary but consistent criterion) by the relation obtained from cancellation of $q\lambda E_m$ between (1) and (2)

$$\tau = H \frac{1}{I_{ds}/W} \left(\frac{I_{sub}}{I_{ds}} \right)^{-\varphi_{it}/\varphi_i} \tag{3}$$

where H (in $\mathrm{As}/\mu\mathrm{m}$) is a constant, and is a function of the channel length, the temperature, the device technology (interface quality, drain doping, etc.), and the criterion used for definition of the lifetime (e.g. 10% decrease in transconductance as used in foundries). While the proportionality constant H varies from case to case, the functional relationship in (3) is most useful in lifetime measurements and predictions, expressed in the form,

$$\frac{\tau I_{ds}}{W} \propto \frac{1}{(I_{sub}/I_{ds})^a} \tag{4}$$

where the exponent $a = \varphi_{it}/\varphi_i$ is defined as the ratio of the critical electron energy to generate an interface state, $\varphi_{it} (\sim 3.7 - 4.1$ eV), and the critical energy to produce an electron-hole pair by impact ionization, $\varphi_i (\sim 1.3$ eV) [12], in the range of about $2.9 \sim 3.2$. The ratio of these two critical energies defines the very steep dependence of the lifetime on the substrate current, and is largely independent of temperature.

The question has been raised in the literature, *how can some electrons reach energies that are two to three times higher than the drain source potential difference*? An explanation in terms of the electron-electron scattering has been offered for threshold energy less than 3.7 eV (for example, [13]–[15]). In such a case, device lifetime can be extrapolated by using (3), except that the constant H in (3) would be replaced by a function weakly dependent on I_{ds} and V_{ds} [14].

In PMOS devices, HCE degradation can be caused by interface states (positively-charged donor-like trap), or trapped charges in oxide (either negative charge due to trapped electrons or positive charge due to trapped holes) [16], [17]. A technique for separating the effects of interface states and trapped–oxide charge can be found in [18]. The direction of the threshold voltage change upon stressing would indicate whether the dominant charge is positive or negative [16], [17].

III. Lifetime versus Temperature Due to HCE

A. CMOS in dc Operation: Accelerated Lifetime Measurements

Two different types of measurements were used. One is the conventional accelerated lifetime test where the transistor is placed under a severe electric field stress, to reduce the lifetime due to hot-electron degradation in drain-source current I_{ds} and/or transconductance g_m to a practically observable range, by a drain-source voltage, V_{ds}, considerably higher than the nominal core voltage (in our case, 1.8 V for minimal length of 180 nm). The lifetime under the actual operating conditions is then extrapolated based on (3) and (4). This approach is widely used by industry.

A complementary way to approach the lifetime extrapolation is by measurement of the substrate current I_{sub} as a function of drain-source voltage V_{ds} before and after the stress. The conventional test verifies the canonical very steep slope of the inverse relation between the lifetime and the substrate current, $\tau \propto {I_{sub}}^{-3}$, and the substrate current measurement confirms that *a lifetime margin of several orders of magnitude can be achieved* by reducing V_{ds} and I_{ds}/W (drain-source current density).

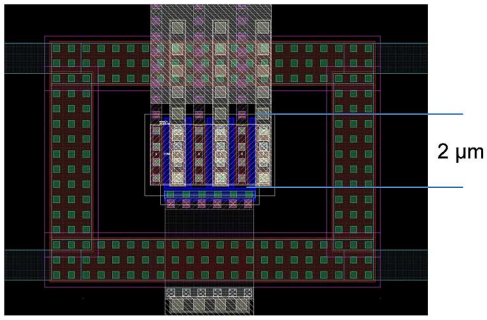

Fig. 2. Layout of a test NMOS transistor, $L = L_{min} = 180$ nm, $W = 10\ \mu$m (5 fingers $\times$ $2\ \mu$m).

The accelerated tests require some care in the design of test transistors. Clearly, the substrate requires a separate contact to allow monitoring of the substrate current. Fig. 2 shows the layout of a test NMOS transistor in a CMOS 180 nm technology, with a length of 180 nm and total width of 10 μm for 5 fingers. The minimal length device was used because it demonstrates the worst-case degradation compared to longer length devices at given stress condition [5]. The test transistors were designed to have negligible voltage drop across parasitic resistance and power dissipation less than 15 mW in stress tests to prevent temperature change due to self-heating.

The stress test flow is shown in Fig. 3 to observe 10% transconductance degradation under drain-source stress voltage from 2.8 V to 3.4 V at room temperature ($\sim$ 300 K) and in liquid Nitrogen ($\sim$ 77 K). The gate-source voltage was set at 1 V both during the stress and in device characteristics measurements, in the region of weak dependence (a broad maximum) of the substrate current on the gate-source voltage. The drain-source voltage in characteristics measurements were set at 1 V to simulate the saturation operation of such devices in the analog front-end ASIC. A device operating in the linear region (e.g. setting $V_{ds} = 50$ mV) would show an apparent larger degradation because the damage is localized at the drain end [19], but operation at such a low V_{ds} is not of interest for the analog front-end ASIC.

B. Results

Fig. 4 shows the measured transconductance degradation of the test NMOS ($L = 180$ nm, $W = 10\ \mu$m) at room temperature and at 77 K in an accelerated lifetime test. Note that in this 180-nm process the 10% g_m degradation at the stress voltage from 2.8 to 3.2 V occurs in the 'saturated' degradation region with slow degradation rate, not in the 'early-mode' region with fast degradation rate. 'Early-mode' degradation exists in LDD (Lightly-Doped Drain) structures commonly used to reduce hot-carrier degradation for submicron CMOS processes [20]. However, the oxide spacer in such a structure introduces additional degradation. In the early stage of hot-carrier stress, degradation is primarily due to the accumulation of negative charge underneath the LDD spacer which increases the parasitic drain series resistance; this increase of series resistance eventually saturates and the degradation is then primarily due to mobility reduction from interface states outside of the LDD region [21]. If in a given CMOS technology 10% g_m degradation takes

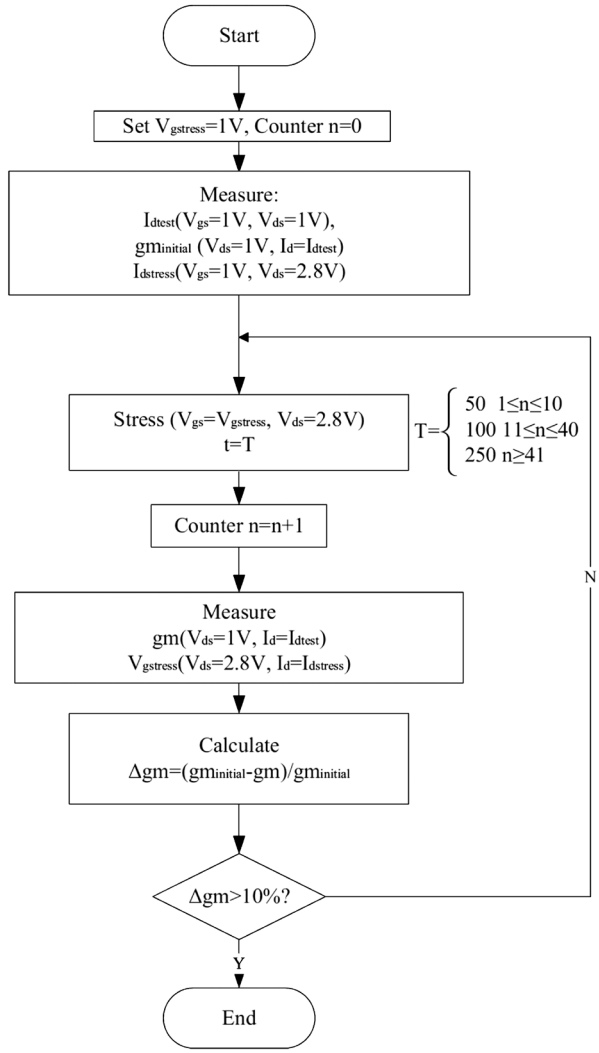

Fig. 3. Stress test flow chart.

place in the early-mode region (for example, [22]), the lifetime prediction should include the effect of the series-resistance increase [21]; if a longer lifetime is required than the one predicted from the early-mode degradation, one may need to design for a tolerance of a larger than 10% g_m degradation.

Upon the measured lifetime in Fig. 4, a stress plot of measured $\tau I_{ds}/W$ at 10% g_m degradation versus I_{sub}/I_{ds} is given in Fig. 5 to verify the characteristic slope for the interface state generation in (4). The measured points at both 300 K and 77 K in Fig. 5 are very close to the theoretical slope, i.e. $a \approx 3$. Although the constant H in (3) would be a function of I_{ds} and V_{ds} at low core voltage [14], in our measurements I_{ds} and V_{ds} vary within a very limited range ($< 5\%$), leaving the characteristic slope largely unaffected.

Common practice in the literature follows the relation in (2), i.e. $\ln(\tau I_{ds}/W) \propto \varphi_{it}/(q\lambda E_m) \propto 1/(V_{ds} - V_{dsat})$, to project the lifetime at the *core voltage* from the stressed points. Since in low-power design the pinch-off voltage V_{dsat} is negligible for moderate and weak inversion in which most analog front-end devices operate, the lifetime versus $1/V_{ds}$ can be approximately projected, as shown in Fig. 6, upon extraction from the stress measurements in Fig. 5. The projected lifetime at 300 K is about

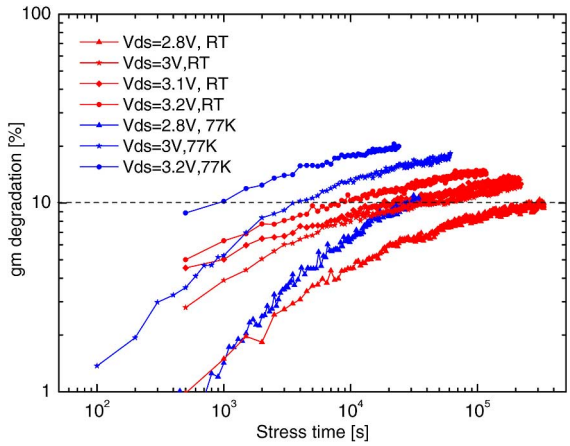

Fig. 4. Measured transconductance degradation versus time of an NMOS transistor ($L = 180$ nm, $W = 5 \times 2$ μm) in accelerated stress tests at room temperature (RT) and at 77 K.

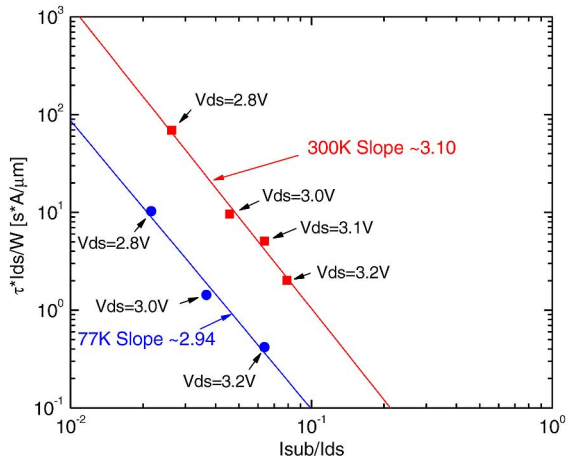

Fig. 5. Measured $\tau^* I_{ds}/W$ versus I_{sub}/I_{ds} for an NMOS transistor of 180-nm length, 10-μm width, and 1.8-V core voltage. The solid lines are plotted to guide the eye and to follow Eq. (4) with $2.9 < a < 3.1$.

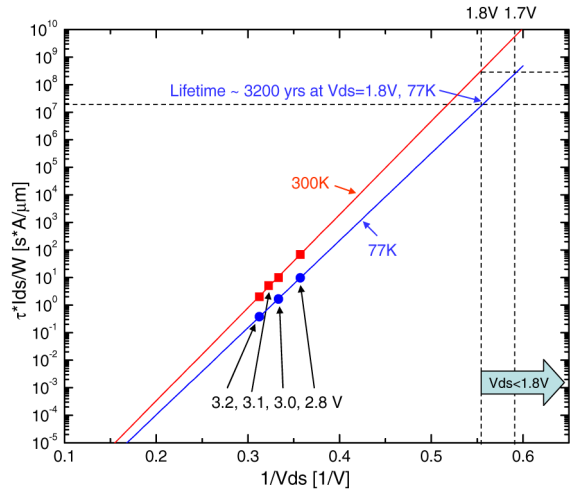

Fig. 6. Projected lifetime vs. $1/V_{ds}$ extracted from the stress measurement results shown in Fig. 5.

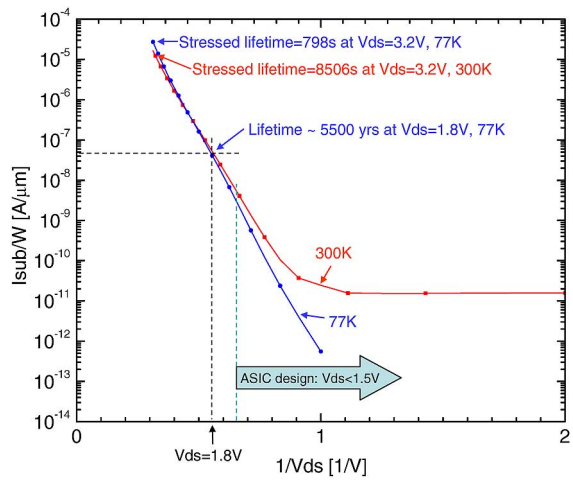

Fig. 7. Measured substrate current density versus $1/V_{ds}$ for an NMOS transistor of $L = L_{\min} = 180$-nm length, 10-μm width, and 1.8-V core voltage. Measured lifetimes under stress, $V_{ds} = 3.2$ V, at 77 K and at 300 K are indicated, as well as extrapolated life time for $V_{ds} = 1.8$ V at 77 K. At $V_{ds} = 1.5$ V, the hot electron degradation for the CMOS 180 nm node becomes negligible for any lifetime of practical interest. (At 300 K the substrate current levels of $\sim 10^{-11}$ A/μm is due to thermal generation.)

an order of magnitude longer than at 77 K. However, *reducing V_{ds} at 77 K only by $\sim 6\%$ makes the lifetime equal to that at 300 K.*

A complementary way to gain some insight into the lifetime extrapolation is by the measurement of the substrate current as a function of V_{ds}. Fig. 7 shows the measured substrate current density versus $1/V_{ds}$, from the highest stress point $V_{ds} = 3.2$ V until it becomes too low to measure. Note that *one order of magnitude in substrate current corresponds to approximately three orders of magnitude in lifetime* in (4), due to $\tau \propto I_{sub}^{-3}$. With the knowledge of I_{sub} over the whole V_{ds} range, the lifetime extrapolated to $V_{ds} = 1.8$ V in this way would be ~ 5500 years. Compared to the result in Fig. 6, the uncertainty ($\sim 50\%$) is due to the steep dependence of lifetime on the substrate current ($\tau \propto I_{sub}^{-3}$), and the spread of substrate current of several samples measured ($\sim 10-20\%$) which results in a spread of 30-60% in the predicted lifetimes. Since the predicted lifetimes are about two orders of magnitude longer than the time of interest for the physics experiments (20-30 years), such an uncertainty in the predicted very long lifetimes is not a concern for practical use. In the low-power analog front-end ASIC for LAr TPC [23], all transistors are well below the nominal core voltage of 1.8 V and at a low substrate current. The distribution of I_{sub}/W and $1/V_{ds}$ of all analog transistors in the ASIC is shown in Fig. 8.

Compared to NMOS, PMOS devices have shown a much slower degradation. In Fig. 9, the PMOS devices under stress voltage from 3 to 3.4 V (as compared to lower stress voltage range for NMOS, 2.8 to 3.2 V), at room temperature and at 77 K, experienced only $\sim 2\%$ degradation at stress time comparable to that in the NMOS stress tests (in Fig. 4), and mainly in the early-mode degradation region, demonstrating much slower degradation in PMOS devices, as expected from the literature (e.g. [9]).

C. Noise Due to HCE

Degradation of device noise, including 1/f and white noise, is another important characteristic that may affect the performance of the analog front-end ASIC. Measured equivalent input noise

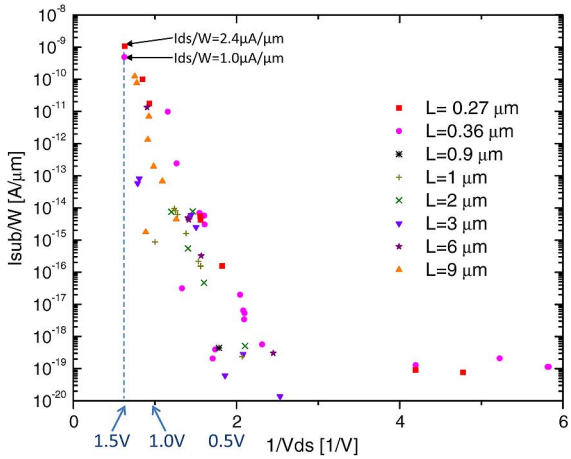

Fig. 8. I_{sub}/W and $1/V_{ds}$ distribution for all transistors in the analog front-end ASIC for LAr TPC [23]. $V_{ds} < 1.5$ V results in a very long extrapolated life time as shown in Fig. 7.

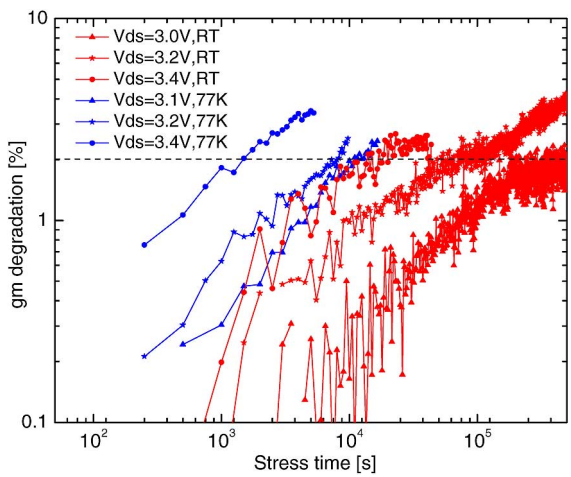

Fig. 9. Measured transconductance degradation of a PMOS transistor ($L = L_{\min} = 180$ nm, $W = 10$ μm) at room temperature (RT) and at 77 K.

for NMOS and PMOS devices before and after stress, at room temperature and at 77 K, are shown in Fig. 10. Both NMOS and PMOS devices have the length of 180 nm and the width of 10 μm. NMOS devices were stressed to 10% (and 15% at 77 K) g_m degradation; while PMOS devices were stressed to 2% (and 3.5% at 77 K) g_m degradation, though requiring a much longer stressing time due to its slower degradation compared to NMOS. It is evident that in the PMOS device the stress has not influenced the noise spectral density much and the 1/f noise is much lower at 77 K than at room temperature. The PMOS device is used as the input MOSFET in the preamplifier and is a dominant noise contributor in the front-end ASIC [23]. The input PMOS transistor is operated at $V_{ds} \sim 200$ mV, where hot carrier effects should be negligible. The much larger g_m degradation in NMOS transistors is accompanied by an increase in 1/f noise. The effect of this on the ASIC overall noise is made negligible by a) the circuit design minimizing the later stage noise contributions, and altogether by b) the circuit design avoiding stress conditions, as shown in Fig. 8.

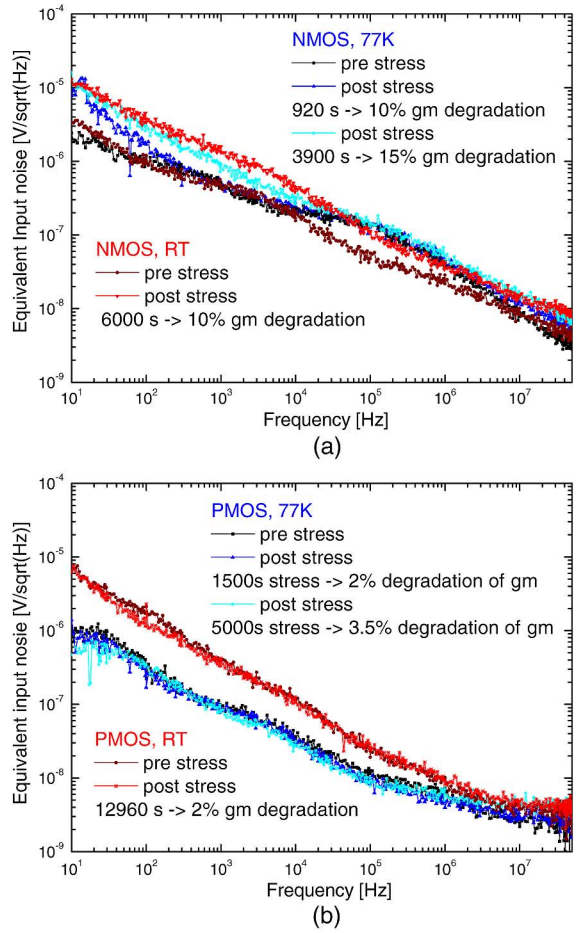

Fig. 10. Measured equivalent input series noise at room temperature and at 77 K for: (a) NMOS before and after being stressed to 10% (and 15% at 77 K) g_m degradation, and (b) PMOS before and after stressed to 2% (and 3.5% at 77 K) g_m degradation, both with size $L = 180$ nm and $W = 10$ μm.

D. CMOS in ac Operation: Logic Circuits and FPGAs

It has been long established [24] that ac and dc hot-carrier induced degradation is the same if the *effective stress time*, t_{eff}, during the switching cycle is taken into account. This quasi-static model, confirmed recently [25], considers the ac stress as a series of short dc stresses, each for a time t_{eff}, strung together. The lifetime of a logic circuit driven at a clock frequency f_{ck} can be related to the lifetime of the NMOS transistor under continuous ac operation in terms of the ratio of the effective stress time during a change of state and the clock period. Thus the lifetime of digital circuits is extended by the inverse duty factor $1/(f_{ck}t_{eff})$, compared to dc operation [24].

A measurable degradation of NMOS devices due to hot-carrier effects occurs only when V_{ds} is close to or above the core voltage and I_{ds} is high. In the switching cycle, that corresponds to a fraction of the gate voltage rise time, which is defined as the effective stress time t_{eff}.

A rough estimation of t_{eff} as 1/4 of the gate voltage rise time for NMOS (while 1/10 of the gate fall time for PMOS) was given in [24]. More detailed estimation can be found in the design manual of major foundries. An accurate estimation requires a calculation of the substrate current during the change of state.

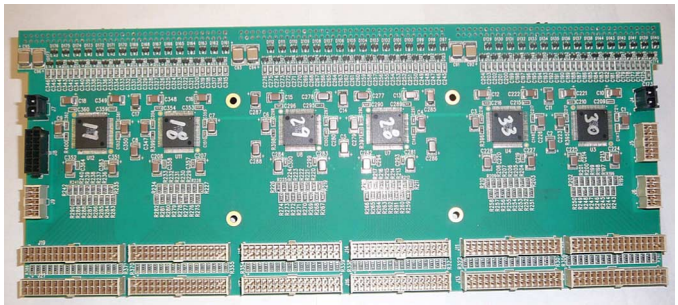

Fig. 11. Cold motherboard with 12 LAr TPC front-end ASICs on both sides of the board (192 signal channels) tested by multiple immersions in liquid nitrogen.

The inverse duty factor $1/(f_{ck}t_{eff})$ is large (> 100) for deep submicron technology and clock frequencies (up to 200 MHz) which may be needed for the TPC readout.

The principal design guideline for digital circuits and FPGAs is to keep the inverse duty factor high. If that is not possible, and as an additional conservative measure, reducing V_{ds} by $\sim 10\%$ would add an order of magnitude margin to the lifetime.

A standard method for accelerated stress testing of FPGAs is to observe ring oscillator frequency under severe V_{ds} stress [26]. Degradation of I_{ds} leads to increased rise (propagation) time and reduced ring frequency. Additional evaluation of FPGAs may be necessary, to verify the lifetime of any circuits not characterized by the ring oscillator test.

IV. Reliability Under Thermal Cycling

Other than the hot carrier effects, reliability under thermal cycling is a very important issue when applying cold electronics to a LAr TPC. We have thus subjected fully assembled circuit boards (including plastic packages, passive components, surface mount solder joints, connectors, etc.) to numerous thermal cycles between 77 K and 300 K. The most severe thermal stress for assemblies of many diverse components is the temperature cycling of completed circuit boards by alternating immersion in liquid nitrogen with bringing to room temperature by hot air. As an example, all $\sim$ 10,000 boards for ATLAS LAr calorimeter [27] have been cycled 5-10 times each. Compared to such testing, operation in LAr is tranquil as evidenced by virtual absence of failures during several experiments involving cold electronics over long periods of time. The risk of failure due to damage during detector assembly is much higher than the risk of device failure during operation.

Fig. 11 shows a cold motherboard with 12 LAr TPC front-end ASICs on both sides. During extensive testing of ASICs and the motherboard, ASICs have gone through a total of $\sim$ 2200 immersions (of multiple chips) in liquid nitrogen, and the board has been immersed $\sim$ 40 times without a single failure.

V. Conclusion

A study of hot-carrier effects on TSMC 180-nm CMOS device lifetime has been performed at 300 K and 77 K, with an intended application for LAr TPC readout. Two different measurements were used: accelerated lifetime measurement under severe electric field stress by V_{ds} while observing degradation in the transistor transconductance, and a separate measurement of the substrate current as a function of $1/V_{ds}$ before and after the stress test. The measurements confirm that below a certain value of V_{ds} a lifetime margin of several orders of magnitude can be achieved for the TSMC 180 nm CMOS transistors at 77 K. The low power ASIC design for LAr TPC falls naturally into this domain, where hot-electron effects are negligible.

Lifetime of digital circuits (ac operation) is extended by the inverse duty factor $1/(f_{ck}t_{eff})$ compared to dc operation. This factor is large (> 100) for deep submicron technology and clock frequencies needed for TPC readout. As an additional margin, V_{ds} may be reduced by $\sim 10\%$ for an order of magnitude increase of lifetime.

Extremely low failure rate (incidence) in ATLAS LAr calorimeter over a long time demonstrates on a large scale that surface mount circuit board technology withstands very well even multiple abrupt immersions in liquid nitrogen applied in board testing, and that the total failure incidence in continuous operation over time is very low.

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